Oct 19th

Note Title 19-10-2011

Recap : Direct Mapped Cache

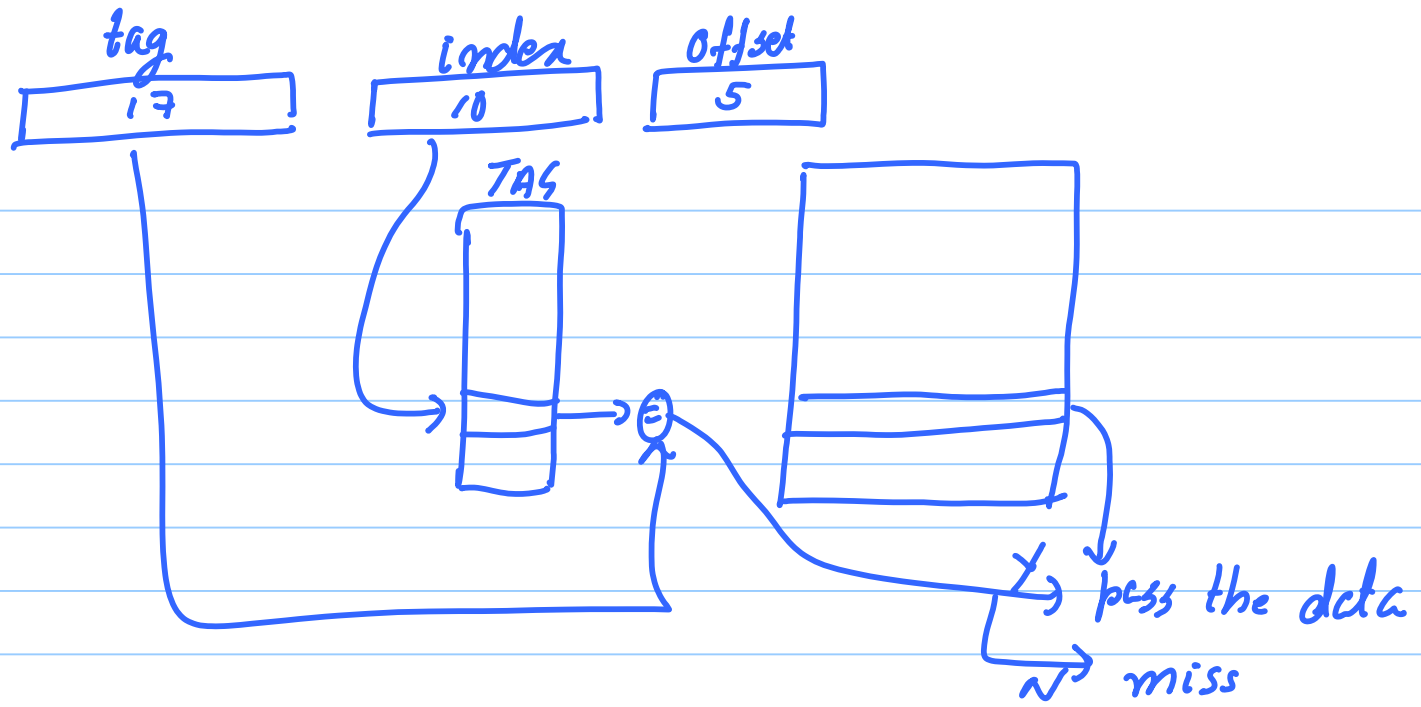
Fully Associative Cache.

One block: 32 bytes.

Size of the cache: 32 kB

Structure of the cache

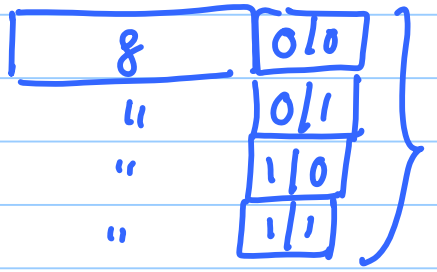
DM

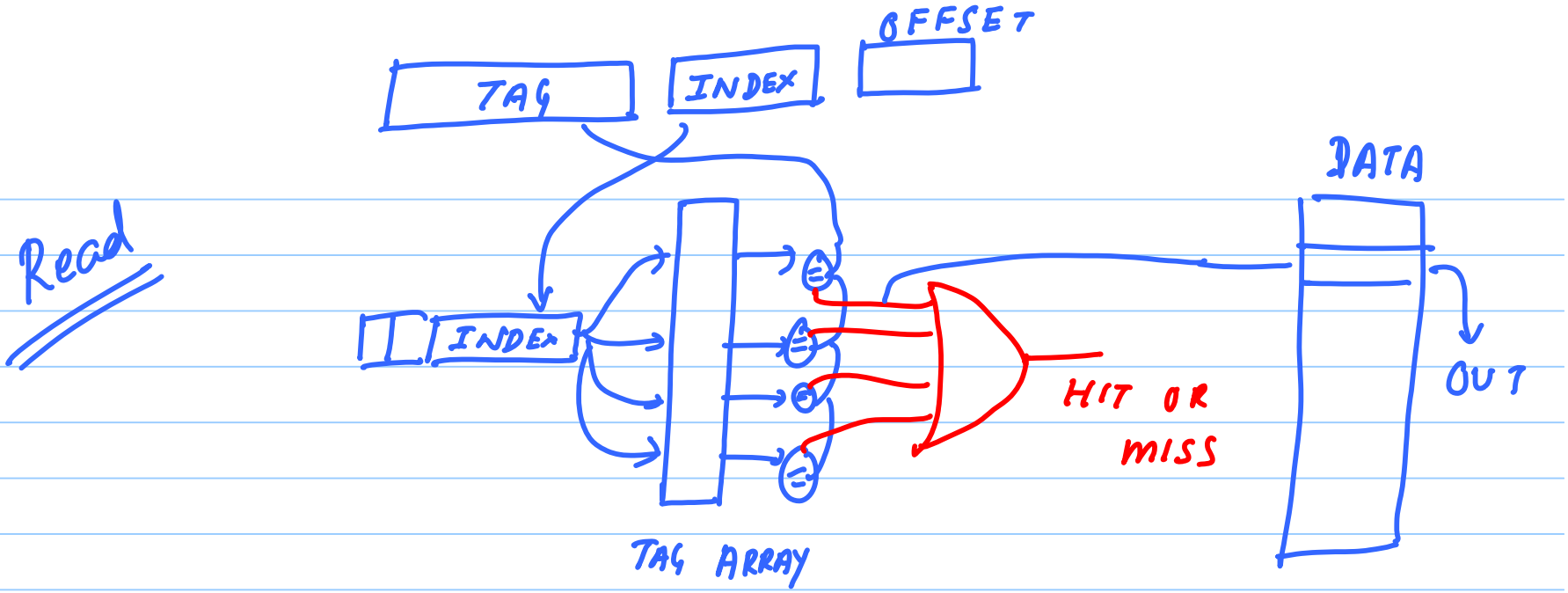


Set Associative Cache

19 8 5

One line can be in 4 locations





Write.

Some extra state per line

V → Valid bit

M → Modified bit

1) Search for a way with V=0

Yes ↓

Write

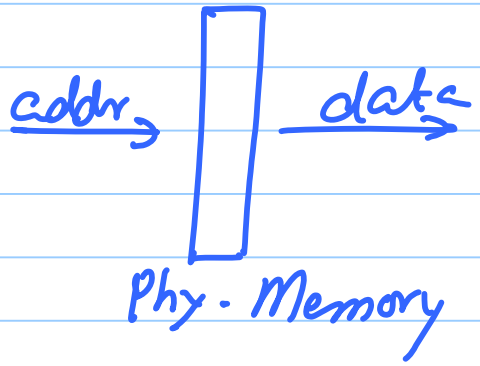
No ↓

Strat. 1) Use LRU replacement policy

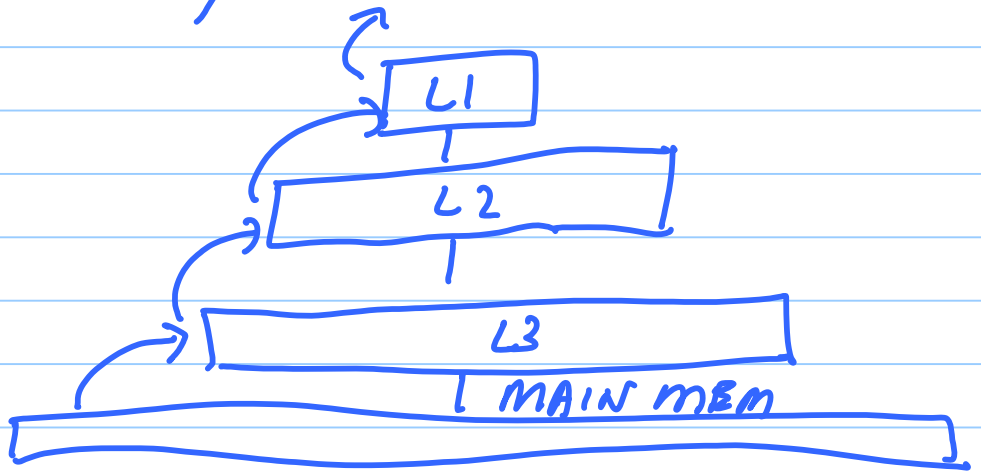
Strat. 2) Give preference to lines with M=0

Cache hierarchy

View from the outside: One unified contiguous physical memory



Insider's View



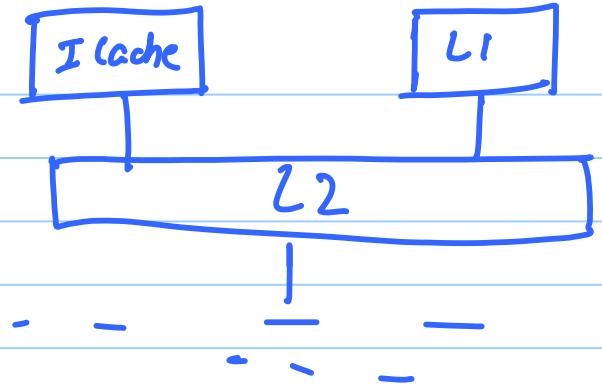
local miss rate: $\frac{\#\text{ of misses at that level}}{\text{total \# of accesses at that level}}$

global miss rate: $\frac{\#\text{ of misses at that level}}{\text{total \# of memory accesses}}$

Three Cs

- Compulsory Miss → cold start
- Conflict Miss → Insufficient ways in the cache
- Capacity Miss → Size of data is larger than the

Realistic Memory Hierarchy cache



What about Writes?

Write Back → Write in L1, set m=1
return
When the line is evicted
if modified write to L2

Write Through → Write to L2 → always
M=0